# This Page Is Inserted by IFW Operations and is not a part of the Official Record

## BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

## IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents will not correct images, please do not report the images to the Image Problem Mailbox.

F-058



H01L 23/56 H01G 1/035 H01L 23/32

#### PATENT ABSTRACTS OF JAPAN

(11) Publication number: 01027251 A

 (43) Date of publication of application: 30 . 01 . 89		
(71) Applicant:	NEC IC MICROCOMPUT SYST	

# 

(21) Application number: 62183888

#### (57) Abstract:

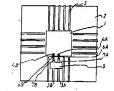
(51) Int. CI

PURPOSE: To reduce inductance, and to prevent the mathunction of a semicenductor device being generated by inductance by directly connecting a capacitor to outer leads for a power supply and a GND in the semiconductor device.

CONSTITUTION: A semiconductor chip 1 with pads 4A, 48 for a GND and a power supely is fined onto a package 2, to which outer leads 3 including outer leads 3A, for the CND and the peower supely are formed and which contakts of ceramics, etc. The paids 4A, 48 for the GND and the power supely are formed and which outer leads 3A 38 for the GND and the power supply bending wrise 6A, 6B, A capacitor 6 is fastered onto the outer leads 3A, 3B, and a terminal 7A for the GND and a terminal 7B for the power supply for the capacitor 5 are diseastly connected respectively to the outer lead 5A for the GND and the outer lead 3B for the power supply Accordingly, inductance is lowered, noises are reduced, and the generation of a maffunction can be prevented.

#### COPYRIGHT: (C)1989, JPO&Japlo

(72) Inventor:



SUDA KOJI